122 126 128 130 132 134 FPGA blocks for User-specific functions and I/O interfaces OPB Master Preprocessor 10/100 FE Peripheral Slave GPIO 106 UART 12C GPIO -166 120 On-chip ipheral (OPB) ARB snq Controller Interrupt 100 Field-Programmable Network Processor Example Controller 118 164 Bridge DMA OPB MAL T = Standard cell logic FIG. 1 116 DDR-SDRAM 160 -Cache II-Cache Controller 400-533 MHz JTAG Trace 440 core MMU (128 bit, 133 MHz) 32b 133 MHz 102 114 MSU|USC Accelerator∄PLB Master∄DDR-SDRAM Controller Alteration Quenes Egress Frame nterface|Interface|Interface|Interface| 112 Processor Local Bus (es) Media 104 154 On-Chip Peripheral Bus Controller 2 Master 170 Media 440 110 152 Mgmnt Header (SRAM) Cache Function-Buffet Media 108 FPGA = FPGA macro(s) Classifier 40 RapidIO _ookup/ Media 150

FIG. 2

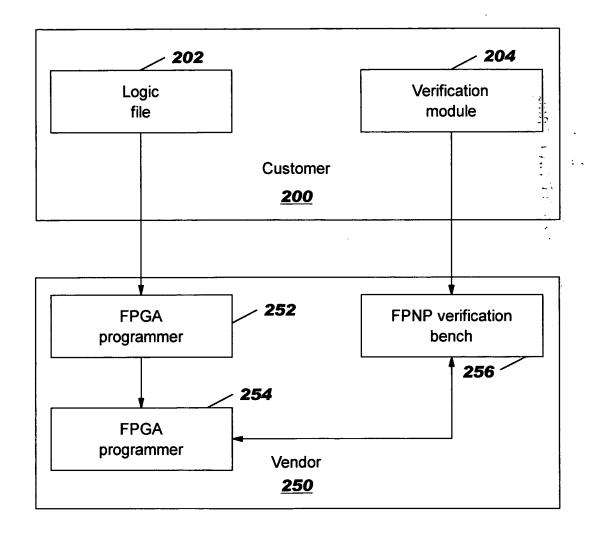


FIG. 3

